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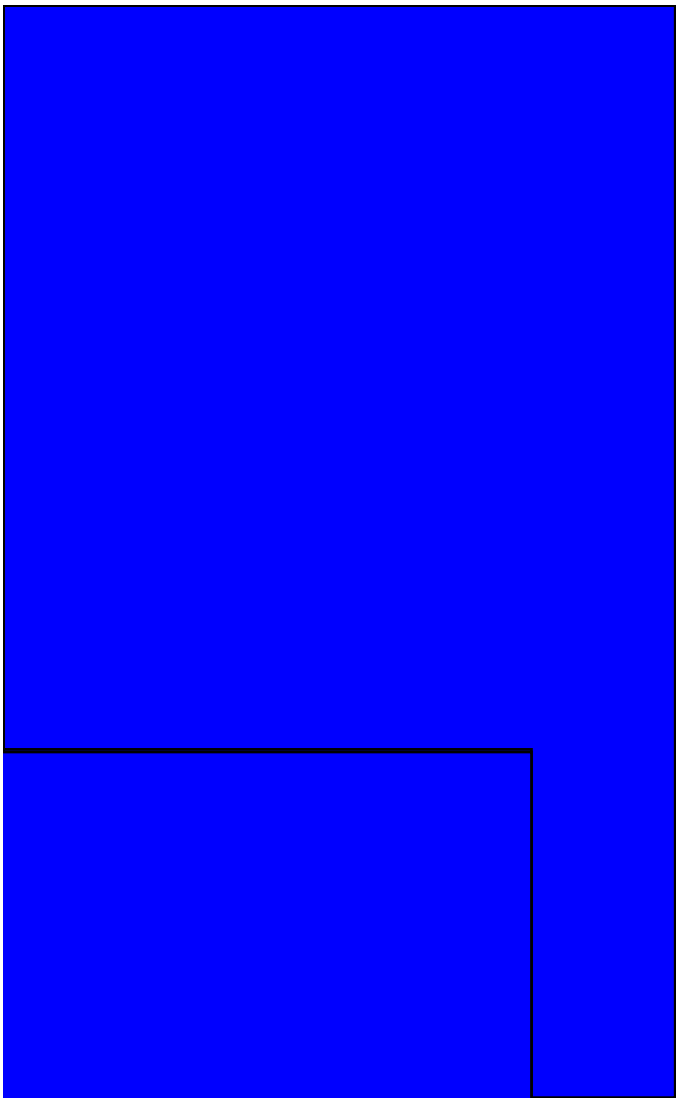

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Revision 1.0: Release to Market

Revision 1.4: Update char and typical application waveforms

Revision 1.5: Update AGND connection of application in page1 and page 12

Revision 1.6: Update DEVICE ORDER INFORĠ TION

Revision 1.7: Update ABS TJ max and add MSL information

ORDERABLE DEVICE	PACKAGING TYPE	STANDARD PACK QTY	PACKAGE MARKING	PINS	PACKAGE DESCRIPTION	MSL
SCT2280FPAR	Tape & Reel	5000	2280	12	QFN2X3-12L	1

Over operating free-air temperature unless otherwise noted(1)

FSEL	4	Switching frequency selection. Connecting to ground sets clock frequency to 400KHz. Floating sets clock frequency to 800KHz. Connecting to VCC sets clock frequency to 1.2MHz.
VOUT	5	VOUT is used to sense the output voltage of the buck regulator. Connect VOUT to the output capacitor of the regulator directly. Keep the VOUT sensing trace far away from the SW node. VIAs should also be avoided on the VOUT sensing trace. A trace larger than 25mil is required.
MODE	6	PFM, USM or FCCM mode selection. Connect the pin to VCC to force the device in Forced Continuous Current Modulation (FCCM) operation mode. Ground the pin to operate the device in Pulse Frequency Modulation (PFM) mode without Ultrasonic Mode (USM). Floating the pin to operate the device in PFM with USM.
SW	7	Connect SW to the inductor and bootstrap capacitor. SW is driven up to VIN through the high-side power MOSFET during on-time. The inductor current drives SW to negative voltage through low-side power MOSFET during off-time. Use wide and short PCB traces to make the connection. Keep the SW pattern area minimized.
BST	8	Bootstrap. Must connect a 0.1uF capacitor or greater between SW and BST to form a floating supply across the gate driver of high-side power MOSFET.
VCC	9	Internal VCC LDO output. The driver and control circuits are powered by VCC. Decouple with 1µF ceramic capacitor placed as close to VCC as possible.
AGND	10	Signal logic ground. AGND is the Kelvin connection to PGND.
FB	11	Feedback voltage Input. Connect FB to the tap of a resistor divider from output voltage to AGND to set up output voltage. The device regulates FB to the internal reference value of 0.6V typical.
EN	12	Enable logic input. EN is a digital input that controls the converter on v † o

(1) SCT provides $R_{\theta JA}$ and $R_{\theta JC}$ numbers only as reference to estimate junction temperatures of the devices. $R_{\theta JA}$ and $R_{\theta JC}$ are not a characteristic of package itself, but of many other system level characteristics such as the design and layout of the printed circuit board (PCB) on which the SCT2280 is mounted, thermal pad size, and external environmental factors. The PCB board is a heat sink that is soldered to the leads and thermal pad of the SCT2280. Changing the design or configuration of the PCB board changes the efficiency of the heat sink and therefore the actual $R_{\theta JA}$ and $R_{\theta JC}$.

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V_{IN}=12V, T_J=-40°C~125°C, typical value is tested under 25°C.

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Power Supply and Output						
V_{IN}	Operating input voltage		4.5		18	V
V_{INUVLO}	Vin UVLO rising threshold		4	4.25	4.45	V
V_{INUVLO_HYS}	VIN UVLO Hysteresis			270		mV
		UN A V, V ' ur ⌠V, 0o ij oaΓb, 0o				
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	Shutrb@m I cerre0t	UN Ů, " eas rr m I ů E0 V ? N				uA

SYMBOL	PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
PG_{TD}	PG low to high delay			0.5		ms
V_{PG}	Power Good PG pull-down strength	I_{PG} =4mA		0.6		V
I_{PG_LEAK}	Power Good PG leakage current	V_{PG}=5V			5	uA
Protection						
I_{LIM_P}	LS MOSFET positive current limit	From source to drain	8.5	10	11.5	A
I_{LIM_N}	LS MOSFET negative current limit	From drain to source, MODE connects to VCC		2.5		A
T_{HICCUP}	Hiccup waiting time			7		ms
V_{OVP_R}	V_{FB} OVP threshold % of V_{REF}	V_{FB} rising		122		%
V_{OVP_F}	V_{FB} OVP threshold % of V_{REF}	V_{FB} falling		117		%
V_{UVP_F}	V_{FB} UVP threshold % of V_{REF}	V_{FB} falling		75		%
T_{SD}	Thermal shutdown threshold	T_J rising		163		°C
	Hysteresis			30		°C

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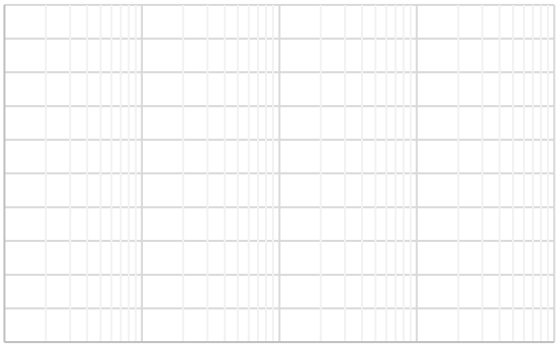

Figure 2. Efficiency vs Iload, Vout=1V, fsw=800kHz

Figure 3. Efficiency vs Iload, Vout=3.3V, fsw=800kHz

Figure 4. Efficiency vs Iload, Vout=5V, fsw=800kHz

Figure 5. Load Regulation, Vout=1V, fsw=800kHz

Figure 6. Load Regulation, Vout=3.3V, fsw=800kHz

Figure 7. Load Regulation, Vout=5V, fsw=800kHz

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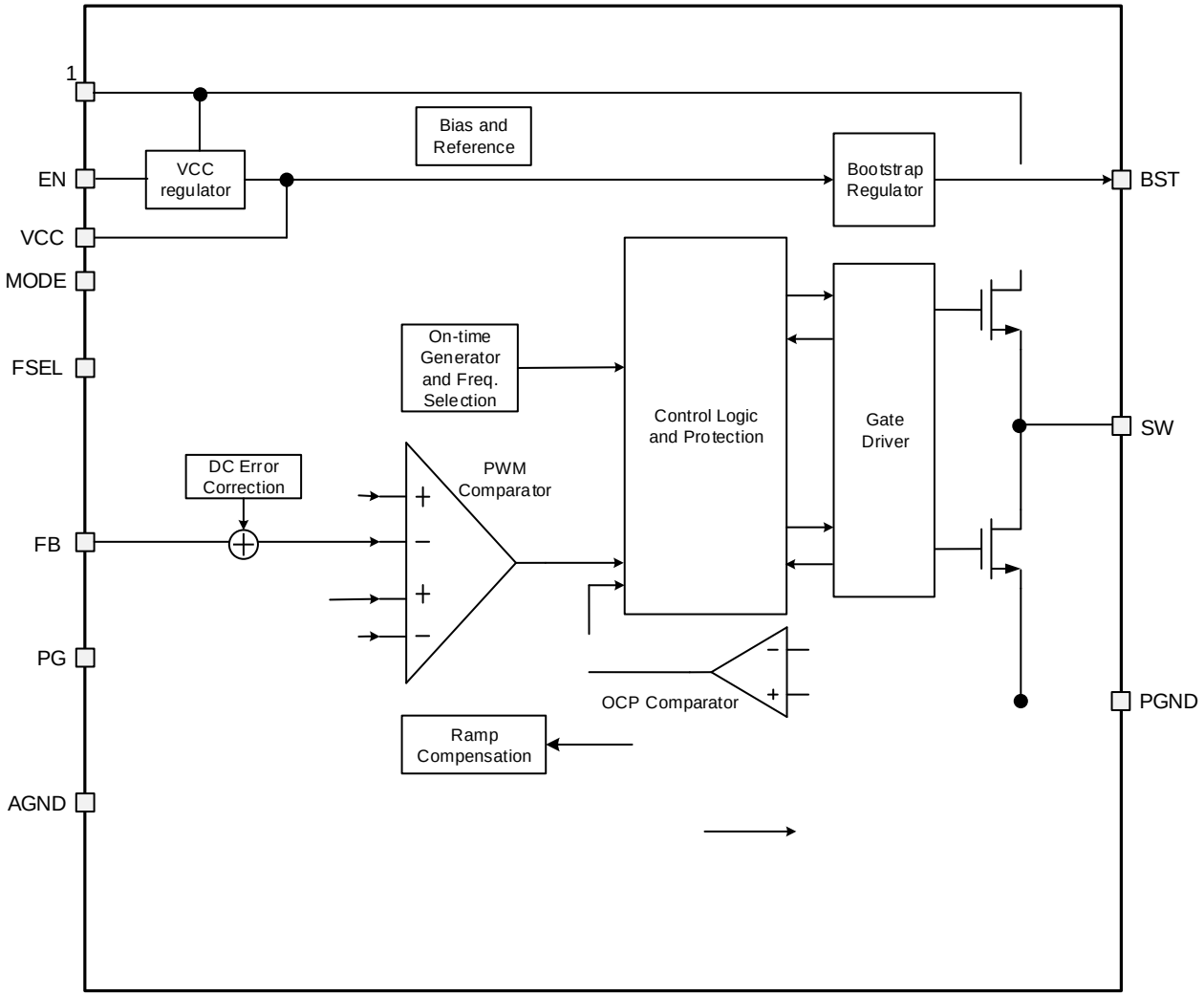

Figure 8. Functional Block Diagram

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Overview

The SCT2280 is a 4.5V-18V input, 8A continuous output synchronous buck converter with built-in 25mΩ

efficiency in light load is much lower than heavy load.

Enable and Under Voltage Lockout Threshold

The SCT2280 is enabled when the VIN pin voltage rises above 4.25V and the EN pin voltage exceeds the enable threshold of 1.18V. The device is disabled when the VIN pin voltage falls below 3.98V or when the EN pin voltage is below 1.1V. An internal 1.5uA pull up current source to EN pin allows the device enable when EN pin floats.

EN pin is a high voltage pin that can be connected to VIN directly to start up the device.

For a higher system UVLO threshold, connect an external resistor divider (R1 and R2) shown in Figure 9 from VIN to EN. The UVLO rising and falling threshold can be calculated by Equation 1 and Equation 2 respectively.

— (1)

— (2)

where

V_{rise} is rising threshold of Vin UVLO

V_{fall} is falling threshold of Vin UVLO

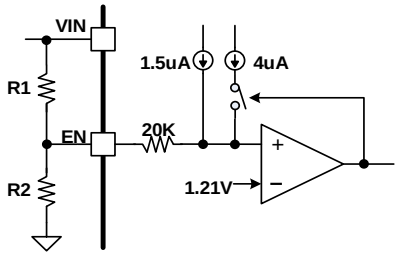

Figure 9. System UVLO by enable divide

Output Voltage

The SCT2280 regulates the internal reference voltage at 0.6V with 1% tolerance over the operating temperature and voltage range. The output voltage is set by a resistor divider from the output node to the FB pin. It is recommended to use 1% tolerance or better resistors. Use Equation 3 to calculate resistance of resistor dividers. To improve efficiency at light loads, larger value resistors are recommended. However, if the values are too high, the regulator will be more susceptible to noise affecting output voltage accuracy.

—— (3)

where

R_{FB_TOP} is the resistor connecting the output to the FB pin.

R_{FB_BOT} is the resistor connecting the FB pin to the ground.

Internal Soft-Start

The SCT2280 integrates an internal soft-start circuit that ramps the reference voltage from zero volts to 0.6V reference voltage in 1ms. If the EN pin is pulled below 1.1V, switching stops and the internal soft-start resets. The soft-start also resets during shutdown due to thermal overloading.

Switching Frequency Selection

The switching frequency of the SCT2280 is selectable to be one of three options: 400KHz, 800KHz and 1200KHz. The switching frequency selel Eq ⁉ ⌋ mMy q ue

Over voltage Protection

The SCT2280 implements the Over-voltage Protection (OVP) circuitry to minimize output voltage overshoot during load transient, recovering from output fault condition or light load transient. The overvoltage comparator in OVP circuit compares the FB pin voltage to the internal reference voltage. When the feedback voltage rises higher than 122% of the feedback voltage, the OVP comparator output goes high and the circuit turns off the HS-FET driver. The LS-FET driver turns on until trigger negative current limit or FB below reference voltage. Then HS-FET turns on with normal ON-time and turn off, following with a LS-FET on until negative current limited triggered or FB lower than reference voltage. The device exits this regulation period when the feedback voltage falls below 117% of the reference voltage.

The SCT2280 offers output discharge under OVP and EN off condition. When OVP is triggered or EN is turn off, a discharge FET is turned on and VOUT pin is connected to a 78Ω discharge resistor.

Thermal Shutdown

The SCT2280 protects the device from the damage during excessive heat and power dissipation conditions. Once the junction temperature exceeds 163C, the internal thermal sensor stops power MOSFETs switching. When the junction temperature falls below 133C, the device restarts with internal soft start phase.

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Typical Application

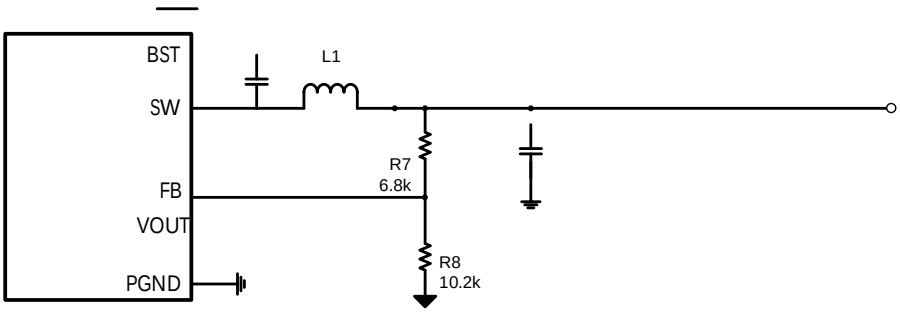

Figure 10. SCT2280 Design Example, 1V Output

Design Parameters

Design Parameters	Example Value
Input Voltage	12V Normal 4.5V to 18V
Output Voltage	1V
Maximum Output Current	8 A
Switching Frequency	800 KHz
Output voltage ripple (peak to peak)	90mV

Input Capacitor Selection

For good input voltage filtering, choose low-ESR ceramic capacitors. A ceramic capacitor 10μF is recommended for the decoupling capacitor and a 0.1μF ceramic bypass capacitor is recommended to be placed as close as possible to the VIN pin of the SCT2280.

Use Equation 4 to calculate the input voltage ripple:

Output Capacitor Selection

The selection of output capacitor will affect output voltage ripple in steady state and load transient performance.

The output ripple is essentially composed of two parts. One is caused by the inductor current ripple going through the Equivalent Series Resistance ESR of the output capacitors and the other is caused by the inductor current ripple charging and discharging the output capacitors. To achieve small output voltage ripple, choose a low-ESR output capacitor like ceramic capacitor. For ceramic capacitors, the capacitance dominates the output ripple. For simplification, the output voltage ripple can be estimated by Equation 7 desired.

(7)

Where

Δ is the output voltage ripple
f_{SW} is the switching frequency
L is the inductance of inductor
C_{OUT} is the output capacitance
V_{OUT} is the output voltage
V_{IN} is the input voltage

Due to capacitor's degrading under DC bias, the bias voltage can significantly reduce capacitance. Ceramic capacitors can lose most of their red a ami

Application Waveforms(Continued)

Unless otherwise noted, the following conditions are VIN=12V, VOUT=1V, Temperature=25C.

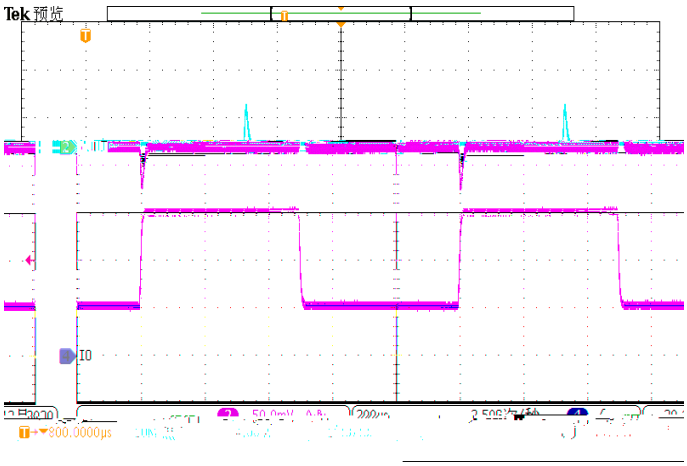

Figure 17. Load Transient (2A-6A, 1.6A/us)

Figure 18. Output Ripple (Iload=0A, PFM)

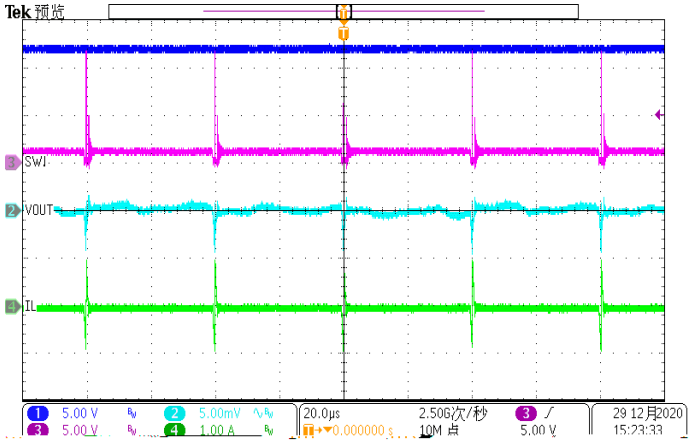

Figure 19. Output Ripple (Iload=0A, USM)

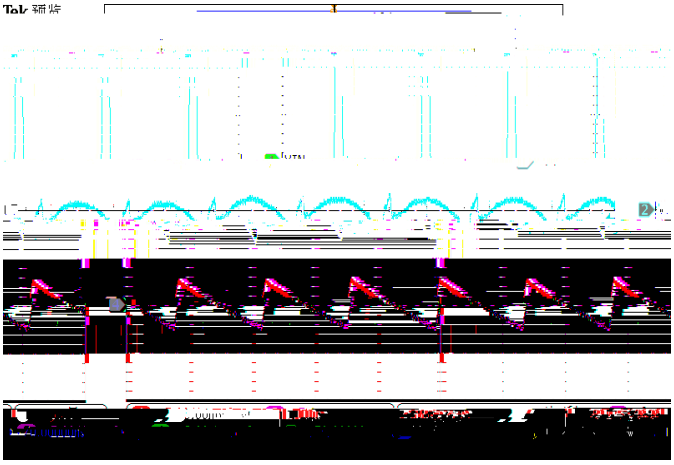

Figure 20. Output Ripple (Iload=0A, FPWM)

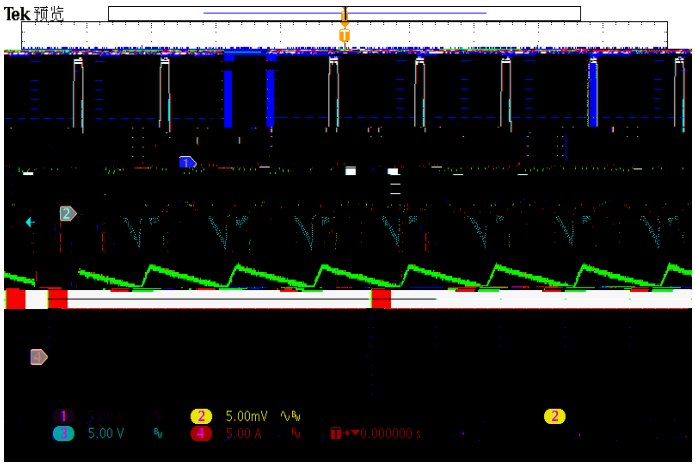

Figure 21. Output Ripple (Iload=8A)

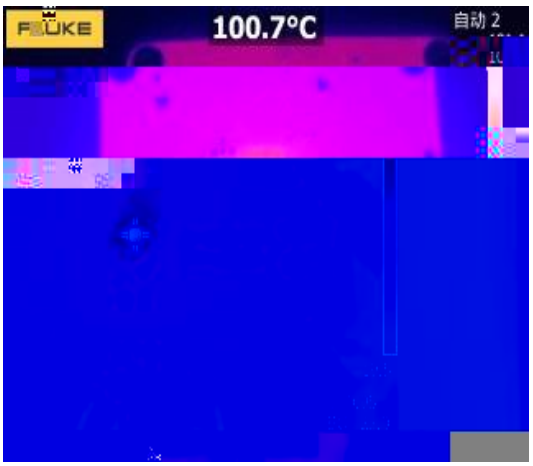

Figure 22. Thermal, 12 VIN, 1 Vout, 8A

Layout Guideline

Proper PCB layout is a critical for SCT2280's stable and efficient operation. The traces conducting fast switching currents or voltages are easy to interact with stray inductance and parasitic capacitance to generate noise and degrade performance. For better results, follow these guidelines as below:

1. Place a low ESR ceramic capacitor as close to VIN pin and the ground as possible to reduce parasitic effect.
2. For operation at full rated load, the top side ground area must provide adequate heat dissipating area. Make sure top switching loop with power have lower impendence of grounding.
3. The bottom layer is a large ground plane connected to the ground plane on top layer by vias. it is recommended 8mil diameter drill holes of thermal vias, but a smaller via offers less risk of solder volume loss. On applications where solder volume loss thru the vias is of concern, plugging or tenting can be used to achieve a repeatable process.
4. Outp

